## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re: Won et al.

Serial No.: To Be Assigned Filed: Concurrently Herewith

Filed: Concurrently Herewith

For: INTEGRATED CIRCUIT

INTEGRATED CIRCUIT CAPACITORS HAVING A DIELECTRIC LAYER BETWEEN A U-SHAPED LOWER ELECTRODE AND A SUPPORT LAYER

Date: September 17, 2003

MS PATENT APPLICATION Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

## REMARKS

Claims 1-7 correspond to Claims 1-7 of the parent application and Claims 8 and 9 correspond to Claims 17 and 20, respectively, of the parent application. Favorable examination and allowance of the present divisional application is respectfully requested. Please note a copy of the certified Korean Application was submitted with the parent application. However, a duplicate copy of the Korean application will be provided upon request.

Respectfully submitted,

Elizabeth A. Stanek Registration No. 48,568

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Date of Deposit: September 17, 2003

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR § 1.10 on the date indicated above and is addressed to: Mail Stop PATENT APPLICATION, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Rosa Lee Brinson